Code No: 137JD

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, December-2023/January-2024
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions

PART – A

(25 Marks)

1.a)	Clearly explain about ION-IMPLANTATION step in IC fabrication.	[2]
b)	Define threshold voltage of a MOS device and explain its significance.	[3]
c)	What are scalable design rules?	[2]
d)	List out the limitations of scaling.	[3]
e)	What are the sources of wiring capacitances?	[2]
f)	What is inverter delay? How delay is calculated for multiple stages?	[3]
g)	List out different applications of SRAM.	[2]
h)	Why refresh operation is required in DRAM?	[3]
i)	List out the commercially available FPGAs.	[2]
j)	What is the need for testing?	[3]

PART – B

(50 Marks)

2.a) Derive an equation for I_D of an n-channel Enhancement MOSFET operating in Saturation region.
b) Explain different forms of pull-ups used as load in CMOS enhancement. [5+5]

OR

3.a) With neat sketch explain BICMOS fabrication in an n-well process.
b) Explain in detail the p-well process for CMOS fabrication indicating the masks used. [5+5]

4. Draw the circuit diagram, stick diagram and mask layout for CMOS two input NOR gate. [10]

OR

5.a) Explain MOS layers with a neat sketch.
b) Explain 2µm CMOS design rule for wires. [5+5]

6.a) Discuss about nMOS transistor as a switch and pMOS transistor as a switch.
b) Define standard unit capacitance. Explain with examples. [5+5]

OR

7.a) Explain the issues involved in driving large capacitor loads in VLSI circuit regions.
b) Calculate the gate capacitance value of 5 mm technology minimum size transistor with gate to channel value is 4×10^{-4} pF/mm^2. [5+5]

8.a) Explain the design of a 4-bit shifter.

b) Discuss the general arrangement of a 4-bit arithmetic process. [5+5]

OR

9.a) Explain the structured design approach of parity generator.

b) Draw and give the design approach for a carry look ahead adder with its structure. [5+5]

10. Draw and explain the block diagram of CPLD. Also list its features. [10]

OR

11. Explain different design strategies for test. [10]

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